Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A computer-implemented method comprising:

determining in a processor whether data in a first portion of a register of the processor has been updated; ~~and~~

if the data in the first portion of the register is updated, setting an indicator bit of an update indicator storage within a second portion of the register to indicate the update; and

if the data in the first portion of the register has not been updated, refraining from transferring the contents of the register back to a memory, based on the indicator bit.

Claim 2 (canceled)

Claim 3 (cancel)

Claims 4 - 5 (canceled)

Claim 6 (previously presented): The method of claim 1 including assigning a single indicator bit as the indicator bit for a plurality of registers, the single indicator bit located in one of the plurality of registers.

Claim 7 (currently amended): An article comprising ~~a medium storing machine readable instructions~~ instructions stored in a computer-readable memory that when executed enable a processor-based system to:

determine whether data in a register of a processor of the processor-based system has been updated; ~~and~~

if the data in the register is updated, set an indicator bit of an update indicator storage within the register to indicate the update; and

refrain from transferring the contents of the register back to a memory if the data in the register has not been updated.

Claim 8 (canceled)

Claim 9 (cancel)

Claims 10 - 11 (canceled)

Claim 12 (currently amended): The article of claim 7 further storing instructions that enable the processor-based system to save the contents of a plurality of registers to [[a]] the memory if the indicator bit is set.

Claim 13 (currently amended): A processor comprising:

a register; and

a storage storing instructions executed by the processor to determine whether the register has been updated and if the register is updated, set an indicator bit within an update status storage within the register, and save the contents of the register to a memory.

Claim 14 (canceled)

Claim 15 (currently amended): The processor of claim 13 wherein said storage stores instructions that enable the processor to refrain from transferring the contents of the register back to [[a]] the memory if the register has not been updated.

Claim 16 (cancel)

Claim 17 (currently amended): The processor of claim [[16]] 13 wherein said storage stores instructions that enable the processor to save the register contents to the memory on a context change.

Claim 18 (canceled)

Claim 19 (previously presented): A system comprising:

a processor having a register;

a storage to store instructions for execution by the system to determine whether the register has been updated and if the register has been updated, set an indicator bit within an update status storage within the register and to not transfer contents of the register to a memory on a context change if the indicator bit is not set;

the memory; and

an interface coupled between said memory and said processor.

Claim 20 (canceled)

Claim 21 (canceled)

Claim 22 (previously presented): The system of claim 19 wherein said storage stores instructions that enable the processor to refrain from transferring the contents of the register back to the memory via the interface.

Claim 23 (previously presented): The system of claim 19 wherein said storage stores instructions that enable the processor to determine whether the register has been updated and if so, save the contents of the register to the memory.

Claim 24 (previously presented): The system of claim 19 wherein said storage stores instructions that enable the processor to save the register contents to the memory on the context change if the indictor bit is set.

Claim 25 (canceled)

Claim 26 (previously presented): The system of claim 19 including a control register to store said indicator bit and wherein said storage to store instructions and said control register are part of said processor.

Claim 27 (canceled)

Claim 28 (currently amended): The method of claim 1, further comprising not saving the register contents to [[a]] the memory on a context change if the register has not been updated.

Claim 29 (canceled)

Claim 30 (canceled)

Claim 31 (previously presented): The processor of claim 13, wherein said register comprises a control register.

Claim 32 (canceled)

Claim 33 (previously presented): The system of claim 19, wherein said register comprises a control register.

Claim 34 (previously presented): The method of claim 1, further comprising:

determining if a context switch occurs; and

clearing the indicator bit upon occurrence of the context switch, then determining whether the first portion of the register has been updated.

Claim 35 (currently amended): The method of claim [[3]] 1, further comprising reducing power consumption of a battery-operated device including the processor by refraining from transferring the register contents.

Claim 36 (previously presented): The method of claim 1, wherein the register comprises a control register, and further comprising setting a main indicator bit of an update indicator storage within a second portion of a main register if a first portion of the main register is updated.

Claim 37 (previously presented): The article of claim 7 further storing instructions that enable the processor-based system to:

determine if a context switch occurs; and

clear the indicator bit upon occurrence of the context switch, then determine whether the register has been updated.

Claim 38 (previously presented): The article of claim 7, wherein the register comprises a control register, and further comprising instructions that enable the processor-based system to set a main indicator bit of an update indicator storage within a main register if the main register is updated.

Claim 39 (previously presented): The processor of claim 13, wherein the storage further stores instructions to:

determine if a context switch occurs; and

clear the indicator bit upon occurrence of the context switch, then determine whether the register has been updated.

Claim 40 (previously presented): The processor of claim 13, wherein the register comprises a control register, and wherein the storage further stores instructions to set a main indicator bit of an update indicator storage within a main register if the main register is updated.

Claim 41 (previously presented): The processor of claim 16, wherein said storage stores instructions that enable the processor to save the contents of the register to the memory through an interface coupled between the processor and the memory.

Claim 42 (previously presented): The system of claim 19, wherein the system comprises a portable system to operate on battery power.

Claim 43 (previously presented): The system of claim 42, wherein the system is to reduce power consumption by refraining from transferring the register contents to the memory on the context switch based on the indicator bit.

Claim 44 (previously presented): The method of claim 6, further comprising setting the single indicator bit if the contents of any of the plurality of registers has been updated.

Claim 45 (currently amended): The method of claim 44, further comprising not transferring the contents of any of the plurality of registers to [[a]] the memory if the single indicator bit has not been updated, otherwise transferring the contents of all of the plurality of registers to the memory.